2.5D silicon interposer and 3D platform for sensors and electronics integration

In a smart sensor microsystem, high sensitivity sensors are used to sense the ambient. A number of physical domains that are often of interest and importance include pressure, acceleration, rotation, etc. These analog signals (potential, capacitive, etc) are often very small in the range of micro-volt or femto-farad. Sensed signals must be conditioned by the CMOS interface electronics that consist of amplifier, filter, ADC and DSP so that the output digital signal can be used by the external world. This is schematically depicted in Fig. 1 below.

![Figure 1: Smart sensor microsystem with the sensing and interface elements.](image)

There exist a myriad of methods for CMOS and sensor integration to realize a smart microsystem such as single chip monolithic approach or multi-package board approach. While monolithic integration offers the best in terms of performance, power and functionality, this method is highly complex and expensive with long time-to-market. On the other end, CMOS and sensor chips can be individually packaged or co-packaged. While this method is low cost, one compromises the system performance and needs to put up with high power consumption due mostly to the extra parasitic loads presented by the external wire bond interconnect. An emerging method for CMOS-sensor integration that can potentially reap the best merits of both monolithic and package implementations is 2.5D silicon interposer or 3D stacking.

Broadly, the main objective of this project is to implement 2.5/3D integration of sensors and electronics (Fig. 2) that satisfy form factor, performance, power consumption, modularity and cost requirements. CMOS readout circuit is stacked on MEMS accelerometer using face-to-face direct metal bonding (Fig. 3). Inter-chip wire bonding is eliminated hence providing small form factor and power consumption. The CMOS chip acts as active cap and provides interconnect routing to the MEMS chip. Metal bonding was achieved at 300oC/10min/50N. Helium leak test suggests that the metal hermetic seal is not degraded after reliability tests. The stacked CMOS/MEMS chip is verified to be functional.
Figure 2: 3D stacking of MEMS sensor and CMOS.

Figure 3: The CMOS chip is bonded face to face on the MEMS chip. The bonded chip is then wire bonded to the package for electrical testing. The vertically stacked CMOS and MEMS chip has a thickness of 1155µm.